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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,064	05/09/2005	Wolfgang Buhr	DE 010359	7154

24737 7590 02/22/2007
PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
STEVENS, THOMAS H	
ART UNIT	PAPER NUMBER
2121	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/500,064	BUHR ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 were examined.

Specification

2. The disclosure is objected to because of the missing headers.

Appropriate correction is required.

3. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicants' use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.

(b) CROSS-REFERENCE TO RELATED APPLICATIONS.

(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.

(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.

(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.

(f) BACKGROUND OF THE INVENTION.

(1) Field of the Invention.

(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.

(g) BRIEF SUMMARY OF THE INVENTION.

(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).

(i) DETAILED DESCRIPTION OF THE INVENTION.

(j) CLAIM OR CLAIMS (commencing on a separate sheet).

(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).

(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-12, 14 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Lasker et al., (US Patent 5,586,291; hereafter Lasker). Lasker teaches a disk controller with volatile and non-volatile cache memories (title).

Claim 1. A method for writing to NV memories (column 18, lines 15-18) in a controller (column 18, lines 35-39) architecture, characterized in that (a) defined data value(s) or (a) defined data word(s) (column 5, lines 32-34)is/are written to (a) defined destination address(es) within the NV memory, by writing the data value(s) (column 18, lines 15-18) or the data word(s) to the predetermined position (data originally in the host computer, column 3, lines 8-11) of the cache page (cache memory, column 3, lines 65-67) register of the NV memory and updating the page address pointer (columns 9-10, lines 60-67, 1-2, respectively; "update or invalidate the data in both volatile and NV memories" column 3, lines 40-47) registers of the NV memory.

Claim 2. A method as claimed in claim 1, characterized in that, for writing to the NV memory, the instruction set of the controller (column 18, lines 35-39) core is extended by additional move code write instructions (MOVCWR instructions ("other write options", column 5, lines 37-41)).

Claim 3. A method as claimed in claim 1, characterized in that the additional instructions of the controller (column 18, lines 35-39)core perform a transfer of the parameters for address pointers (columns 9-10, lines 60-67, 1-2, respectively; "update

or invalidate the data in both volatile and NV memories" column 3, lines 40-47) and for the data value to be written or the data word to be written and activate corresponding control signals for a memory management unit (MMU) (column 18, lines 35-39)and NV memory interfaces.

Claim 4. A method as claimed in claim 1, characterized in that the address processing for the MOVCWR instructions ("other write options", column 5, lines 37-41) is performed in the same way as the processing of code fetches or MOVC instructions, in the presence of a memory management unit (MMU) (column 18, lines 35-39).

Claim 5. A method as claimed in claim 1, characterized in that this MMU is extended by a control signal path in the presence of a memory management unit (MMU) (column 18, lines 35-39)of the controller.

Claim 6. A method as claimed in claim 1, characterized in that, in the presence of an MMU (column 18, lines 35-39), only address areas of the NV memory are written to which have been enabled by the MMU (column 18, lines 35-39).

Claim 7. A method as claimed in claim 1, characterized in that special mapping of the code memory is taken into account within the address area of the controller (column 18, lines 35-39) in the presence of an MMU (column 18, lines 35-39).

Claim 8. A method as claimed in claim 1, characterized in that a plurality of data values and/or data words with the same page address are written in succession (inherent property of memory management, column 18, lines 35-39) .

Claim 9. A method as claimed in claim 1, characterized in that the content of the cache page (cache memory, column 3, lines 65-67) register is programmed into the NV memory by writing to the control register of the NV memory.

Claim 10. A method as claimed in claim 1, characterized in that the cache page (cache memory, column 3, lines 65-67) register of the NV memory is cleared when changing to a new page address in the event of an MOVCWR instruction ("other write options", column 5, lines 37-41).

Claim 11. A method as claimed in claim 1, characterized in that undesired programming of old page register contents under incorrect addresses ("preventing corruption of data in disk storage system" column 3, lines 44-47) is prevented.

Claim 12. An arrangement having a processor, which is designed in such a way that writing to NV memories (column 18, lines 15-18) in a controller (column 18, lines 35-39) architecture may be performed, wherein (a) defined data value(s) or (a) defined data word(s) (column 5, lines 32-34)is/are written to (a) defined destination address(es)

within the NV memory, by writing the data value(s) or the data word(s) to the predetermined position (data originally in the host computer, column 3, lines 8-11) of the cache page (cache memory, column 3, lines 65-67) register of the NV memory and updating the page address pointer (columns 9-10, lines 60-67, 1-2, respectively; "update or invalidate the data in both volatile and NV memories" column 3, lines 40-47) registers of the NV memory.

Claim 14. A computer program product, which comprises a computer-readable storage medium, on which a program is stored which, once it has been loaded into the memory of a computer or of a smart card controller (column 18, lines 35-39), allows the computer or smart card controller to perform writing to NV memories (column 18, lines 15-18) in a controller architecture, wherein (a) defined data value(s) or (a) defined data word(s) (column 5, lines 32-34) is/are written to (a) defined destination address(es) within the NV memory, by writing the data value(s) or the data word(s) to the predetermined position of the cache page register (cache memory, column 3, lines 65-67) of the NV memory and updating the page address pointer (columns 9-10, lines 60-67, 1-2, respectively; "update or invalidate the data in both volatile and NV memories" column 3, lines 40-47) registers of the NV memory.

Claim 15. A computer-readable storage medium, on which a program is stored which, once it has been loaded into the memory of a computer or of a smart card controller, allows the computer or smart card controller (column 18, lines 35-39)to perform writing to NV memories (column 18, lines 15-18)in a controller architecture,

wherein (a) defined data value(s) or (a) defined data word(s) is/are written to (a) defined destination address(es) within the NV memory, by writing the data value(s) or the data word(s) to the predetermined position of the cache page register (cache memory, column 3, lines 65-67) of the NV memory (column 18, lines 15-18)and updating the page address pointer registers of the NV memory.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sowards, titled "Non-Volatile Memory: The Principles, the Technologies, and their Significance to the Smart Card Integrated Circuit", (hereafter Sowards) in view of Lasker.

Per claim 13 Sowards teaches

- Smart Card (title and introduction)

Therefore it would have been obvious to a person having ordinary skill in the art at the time of applicant(s) invention to modify Sowards in view of Lasker because Lasker allows the non-volatile memory to be made rapidly available and increase efficiency (column 5, lines 37-41).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicants' disclosure:

- Ratchev-D., "Are NV--Memories Non-Volatile?" IEEE 1993, pg. 102-106; teaches enhancements of the quality and reliability of newer NV-memory.
- Chen et al., "Write Caching in Distributed File Systems" IEEE 1995 pg. 457-466; teaches trace-driven simulation experiments to write caching in distributed systems with both volatile and non-volatile caches.

- Sowards-D., "Non-Volatile Memory: The Principles, the technologies, and their significance to the smart card integrated circuit". Emosyn and Silicon Storage Technology.6/25/01 pg. 1-14: teaches an introduction to the subject of smart cards and non-volatile memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (7:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Anthony Knight 571-272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

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